Project profile

Cluster for Application and Technology Research in Europe on NanoElectronics

CT206 | Ultimate enablement research on 32/28nm CMOS technologies [UTTERMOST]

PROJECT CONTRIBUTES TO

Communication	✔
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	✔
Digital lifestyle	✔
Design technology	✔
Sensors and actuators	
Process development	✔
Manufacturing science	✔
More than Moore	
More Moore	✔
Technology node	32/28 nm

PROCESS DEVELOPMENT

Partners:

Alcatel-Lucent
Cameca
CEA-INAC
CEA-LETI
CNRS-LTM
CNRS/CEMES
Dolphin
Fraunhofer Institutes
GLOBALFOUNDRIES
IBS
INPG/IMEP
Intel Mobile Communications (formerly Infineon Technologies)
Serma Technologies
ST-Ericsson
STMicroelectronics
Thales Communications
Uni Stuttgart

Project leader:

Gilles Thomas
STMicroelectronics

Key project dates:

Start: January 2010 (June 2010 for German partners)
End: May 2013

Countries involved:

France
Germany

The UTTERMOST project is setting out to transform earlier research into a fully-fledged technology platform to enable the design and cost-effective manufacture of 32/28 nm technology in Europe. The consortium of major chipmakers, equipment manufacturers and research institutes will generate advanced process modules and validate a design platform for reliable 32/28 nm digital and memory technologies on 300 mm wafers in two European manufacturing facilities based on four product demonstrators designed by three application providers. UTTERMOST will thus strengthen the competitiveness of European industry by providing complete solutions for low-power communications-centred multi-core architectures.

Traditionally, the introduction of a new European CMOS technology node is carried out in two phases. The first is the early research that leads to demonstration of the integration of a transistor-based architecture and a proof of concept on a static random access memory (SRAM) cell. The second is the development phase leading to production and industrialisation.

The CATRENE CT206 UTTERMOST project is focusing on this second phase for the deployment of 32/28 nm technology. It brings together a consortium of specialists from across the European semiconductor industry. These include leading chipmakers keen to collaborate on the development of the latest core CMOS technology platform including design kit, models, and libraries and, in parallel, deploy the technology at design and manufacturing level.

Fully-fledged platform

UTTERMOST is making use of earlier 32 nm research performed in the FP6 PULLNANO project, which provided an initial demonstration of a 32 nm SRAM, and by the IBM International Semiconductor Development Alliance (ISDA). It will continue the 32 nm development effort in Europe up to full production and industrialisation. This Phase 2 effort is a multi-year, large resource investment to transform initial research into a fully-fledged technology platform enabling the design of semiconductor products and their cost-effective manufacture in Europe.

The CATRENE project is more than process flow transfer. It involves enabling a technology platform and using that platform to demonstrate products and their high yield in production. Three systems companies have joined the consortium to design complex demonstrators in 32/28 nm, prefiguring future commercial products. It is anticipated that most effort will go directly towards manufacturing commercial products based on a 28 nm technology platform.

By mainly targeting the 28 nm node, UTTERMOST intends to attain the leading edge of international competition. Indeed, at world level, when the CATRENE project was approved, no competitor had yet announced a production-worthy 28 nm technology platform. By trying for an extra half node beyond 32 nm, the CATRENE project has the objective of projecting Europe to the forefront of the global semiconductor industry.

Double validation required

Enabling a technology platform is taking an increasing share of the cost of developing a technology node. At the 32 nm level, the development in terms of design and validation of a complete offer of libraries represents 50% of the overall human-resource-related cost of the new technology.

Complete design enablement of a 32/28 nm technology node will well require some hundreds of person years because validations are required individually for the 32 nm version and then for the 28 nm version.

Product demonstration

R&D effort does not stop at platform level. In fact, the work required to develop marketable products is around five times higher than that involved in the development of a technology platform. For this reason, the CATRENE project will focus on product demonstrators. For the semiconductor industry, the complexity of designing system-on-chip (SoC) devices at 45 nm caused the product time to market to increase by 32% to 2.3 years.

Technology enablement will be achieved through:

- Test-mask development for process validation;
- Extended library design and modelling;
- Design methodology enhancement and portability/scaling of libraries; and
- Assessment of the integration choices in four major demonstrators.

The three manufacturing partners will contribute to the development of demonstrator chips to characterise, validate and industrialise the 32/28 nm CMOS platform. These demonstrators will contribute to the optimisation of the technology and pave the way for time-to-volume production in a cost-effective manner.

Equipment suppliers are an integral part of the semiconductor ecosystem. They have an in-depth understanding of the way to optimise the wafer-processing steps performed by their equipment. As well as supplying equipment, they will deliver the tailored processing performance and reproducibility required in a semiconductor fabrication unit.

Challenging goals

UTTERMOST's goals are challenging but success will enable technical development capabilities to be proven for 32/28 nm node manufacturability on 300 mm wafers by mid project. From experience in previous MEDEA+ projects, this would leave chipmakers enough time to bring the technology to full industrial exploitation within the time frame predicted by the International Technology Roadmap for Semiconductors for industrial production of the 32/28 nm technology node.

As a result, European players would then be able to propose the most advanced CMOS logic technology for semiconductor product fabrication and maintain their position in the world-wide ranking.

This CATRENE project will contribute to new business development and boost Europe's position for innovative applications, particularly in communications components and chipsets. 32 nm CMOS computing and storage power is seen as the enabler of emerging fourth generation (4G) wireless networks, such as 3.5G HSDPA/HSUPA, WiMAX and 4G LTE/SAE.

Success will also strengthen the position of equipment suppliers and enable them to expand further their product portfolio for silicon industry applications. Research organisations and academic teams will gain intellectual property and process module knowledge on industrial lines, enabling them to extend their influence and draw interest from other industrial partners.

Ample opportunities

UTTERMOST will thus provide ample opportunities for European companies to continue participating in the most advanced high speed interfaces for new product creation. Such products will power portable devices that will define a wireless century characterised by pervasive broadband wireless communications and networking.

This transformation is being driven by an explosion in bandwidth-intensive multimedia applications, as well as by the expanded technological capabilities of personal communications systems, air interface technology, IP networking and new architectures, such as mesh networking.

CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

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